Abstract of the Disclosure

A packet processing circuit includes a plurality of macros and a clock supply unit. Each of the macros processes packet data on the basis of a clock and outputs the processed packet data from at least one route. The macros are cascade-connected. The clock supply unit supplies the clock to a macro to be controlled and, when no packet data is output for a predetermined time from all routes of a macro on the input side of the macro to be controlled, stops supplying the clock to the macro to be controlled.